Patent claims

1. A method for fabricating a short channel field-effect transistor, comprising the steps of:

a) preparing a semiconductor substrate (1);

b) forming a first mask layer (2) at the surface of the semiconductor substrate (1);

c) lithographically patterning the first mask layer (2) to form a first mask (2BM) with substantially perpendicular side walls;

d) carrying out a chemical conversion of at least one side wall of the first mask (2BM) to form a sublithographic mask layer (3);

e) lithographically patterning the sublithographic mask layer (3) to form a sublithographic gate sacrificial layer (3M);

f) removing the first mask (2BM);

g) forming spacers (7S, 7S') at the side walls of the sublithographic gate sacrificial layer (3M);

h) forming connection regions (LDD) and/or source/drain regions (S, D) in the semiconductor substrate (1);

i) forming a sacrificial filling layer (8) to embed the sublithographic gate sacrificial layer (3M) and the spacers (7S);

j) removing the sublithographic gate sacrificial layer (3M) to form a gate recess;

k) forming a gate dielectric (10) in the gate recess;

l) forming a control layer (11) in the gate recess;

m) removing the sacrificial filling layer (8) in order to uncover the source/drain regions (S, D);

n) forming connection layers (12) for the source/drain regions (S, D); and

o) forming an insulation layer (13) in order to level a semiconductor surface.

2. The method as claimed in patent claim 1, characterized by the further steps of:

e1) forming a protective layer (4) for the sublithographic mask layer (3) before step e); and
e2) removing the protective layer (4) after step e).

3. The method as claimed in patent claim 2, characterized in that in step e1) the protective layer (4) is formed over the entire surface of the sublithographic mask layer (3) and is then caused to recede as far as the sublithographic mask layer (3).

4. The method as claimed in one of patent claims 1 to 3, characterized in that in step d) a conformal conversion of the side walls of the first mask (2BM) is carried out over a thickness range of from 5 to 50 nanometers.

5. The method as claimed in one of patent claims 1 to 4, characterized in that the first mask layer (2) includes a semiconductor material, and the chemical conversion in step d) represents an oxidation of the semiconductor material.

6. The method as claimed in patent claim 5, characterized in that in step d) a wet oxidation with H_2 and O_2 is carried out.

7. The method as claimed in one of patent claims 1 to 6, characterized in that in steps b) and c)
b1) a first resist layer is formed at the surface of the mask layer (2);
c1) the resist layer is lithographically patterned in order to form a first resist mask (RM); and
c2) the mask layer (2) is patterned using the first resist mask (RM).

8. The method as claimed in one of patent claims 1 to 7, characterized in that the mask layer (2) includes an etching stop layer (2A), and in step e) a second resist mask (5) is used as etching mask.

9. The method as claimed in patent claim 8, characterized in that the first mask layer (2) includes a polysilicon layer (2B) and a silicon nitride layer (2A).

10. The method as claimed in one of patent claims 1 to 9, characterized in that before step g) a further protective layer (6) is formed at the surface of the semiconductor substrate (1), and in step m) this further protective layer (6) is removed again.

11. The method as claimed in one of patent claims 1 to 10, characterized in that in step g) a conformal Si_3N_4 layer (7) is formed and etched anisotropically.

12. The method as claimed in one of patent claims 1 to 11, characterized in that in step h) an ion implantation (I_{LDD}, $I_{S/D}$) with subsequent heat treatment is carried out.

13. The method as claimed in one of patent claims 1 to 12, characterized in that step h) is carried out after step m).

14. The method as claimed in one of patent claims 1 to 13, characterized in that in step i) poly-SiGe is deposited as sacrificial filling layer (8) and planarized.

15. The method as claimed in one of patent claims 1 to 14, characterized in that in step j) the gate sacrificial layer (3M) is removed selectively with respect to the sacrificial filling layer (8) and with respect to the spacer (7S) by wet-chemical means.

16. The method as claimed in one of patent claims 1 to 14, characterized in that in step j) the following additional steps are carried out:

j1) forming a spacer additional layer (9), and
j2) removing a base region of the spacer additional layer (9).

17. The method as claimed in patent claim 16, characterized in that in step j1) conversion of the spacers (7S) is carried out at their surface using atomic oxygen.

18. The method as claimed in one of patent claims 8 to 17, characterized in that in step j) the etching stop layer (2A) is removed in order to uncover the semiconductor substrate (1).

19. The method as claimed in one of patent claims 1 to 18, characterized in that steps k) and l) for filling the gate recess are realized by means of a Damascene process.

20. The method as claimed in one of patent claims 1 to 19, characterized in that in step k) materials with a high dielectric constant are used as gate dielectric (10).

21. The method as claimed in one of patent claims 1 to 20, characterized in that in step l) materials with a high electrical conductivity are used as control layer (11).

22. The method as claimed in one of patent claims 1 to 21, characterized in that in step n) a silicide process is carried out.

23. The method as claimed in one of patent claims 1 to 22, characterized in that step n) is carried out after step h).

24. The method as claimed in one of patent claims 1 to 23, characterized in that the transistor is a PFET and

the control layer (11) includes in-situ boron-doped polysilicon and/or a thin film of boron-doped SiGe followed by polysilicon.

25. The method as claimed in one of patent claims 1 to 23, characterized in that the transistor is an NFET and the control layer (11) includes in-situ arsenic- or phosphorus-doped polysilicon.